

1/8

FIG. 1A(PRIOR ART)

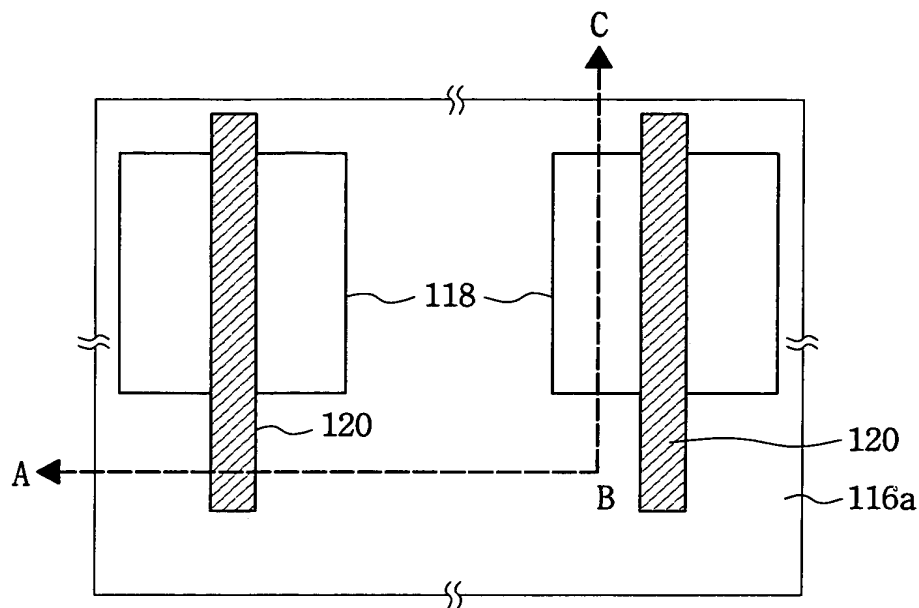
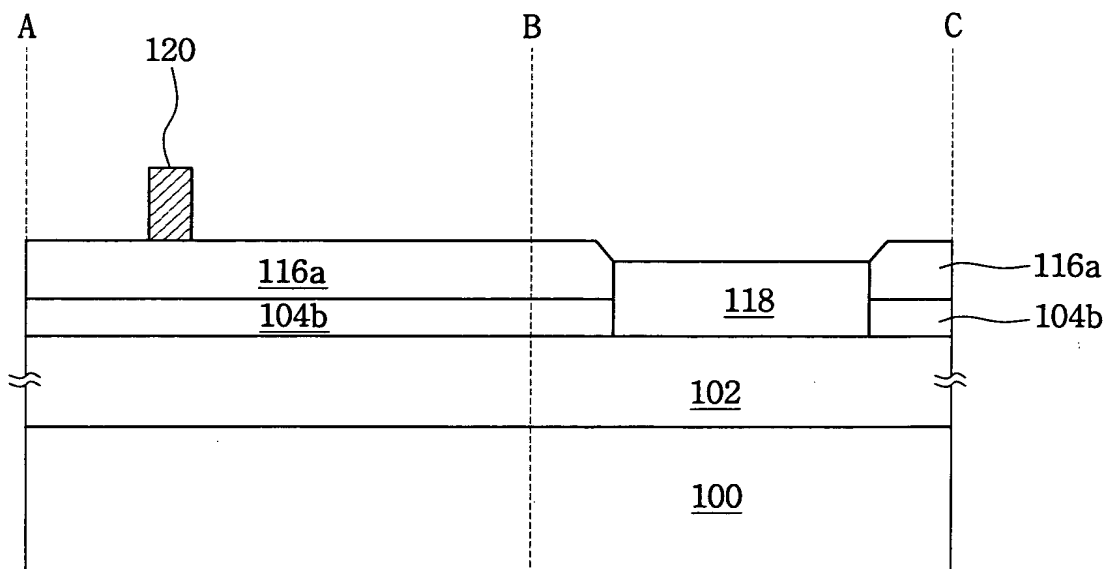


FIG. 1B(PRIOR ART)





A cross-sectional view of a device within a rectangular frame 128. A central channel 120 is filled with a dotted pattern. This channel is flanked by two vertical structures 122, each with a diagonal hatching pattern. Dashed rectangular outlines 118 are positioned on either side of the central channel. A horizontal dotted structure 120 extends from the left side of the frame, passing through the left dashed outline 118. A dashed line with an arrow labeled 'A' points to the left from the end of this horizontal structure. A vertical dashed line with an arrow labeled 'C' points upwards from the top of the central channel 120. A label 'B' is located at the bottom right corner of the central channel. The frame 128 has break lines (double wavy lines) on its top, bottom, and right sides.

This cross-sectional view shows the device structure along line A-A. It features a substrate 100 with a base layer 102. Above the base layer, there is a layer 104b, which is part of a stack including layer 116a. A central region 118 is defined within this stack. A patterned layer 128 is positioned above the central region 118. A layer 122 is located on the top surface, with a thickness 'h' indicated. A small rectangular feature 120 is shown on the left side of the device.

This diagram shows a cross-sectional view of a semiconductor device along line A-A. The device consists of a substrate 100, a first insulating layer 102, and a second insulating layer 104. A conductive layer 106 is formed on the top surface of the second insulating layer 104. A conductive pad 112 is formed on the top surface of the conductive layer 106. The conductive pad 112 is located between points B and C. The conductive layer 106 is located between points A and C. The second insulating layer 104 is located between points A and C. The first insulating layer 102 is located between points A and C. The substrate 100 is located between points A and C. The conductive pad 112 is located between points B and C. The conductive layer 106 is located between points A and C. The second insulating layer 104 is located between points A and C. The first insulating layer 102 is located between points A and C. The substrate 100 is located between points A and C.

This cross-sectional view shows a substrate 100 with a layer 102 on top. A layer 104b is formed on layer 102, and a layer 104a is formed on layer 104b. A gate stack 110 is formed on layer 104a, consisting of a gate dielectric 108 and a gate electrode 112. Five downward arrows are shown above the device, indicating an applied electric field. Vertical dashed lines A, B, and C are shown, with A and C having break symbols at the bottom.

FIG. 4C

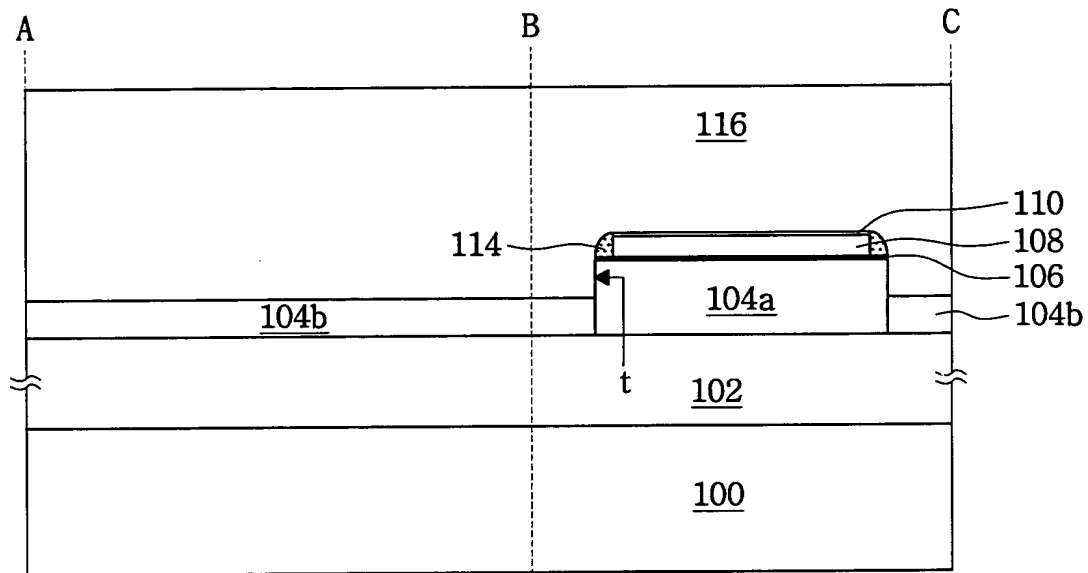
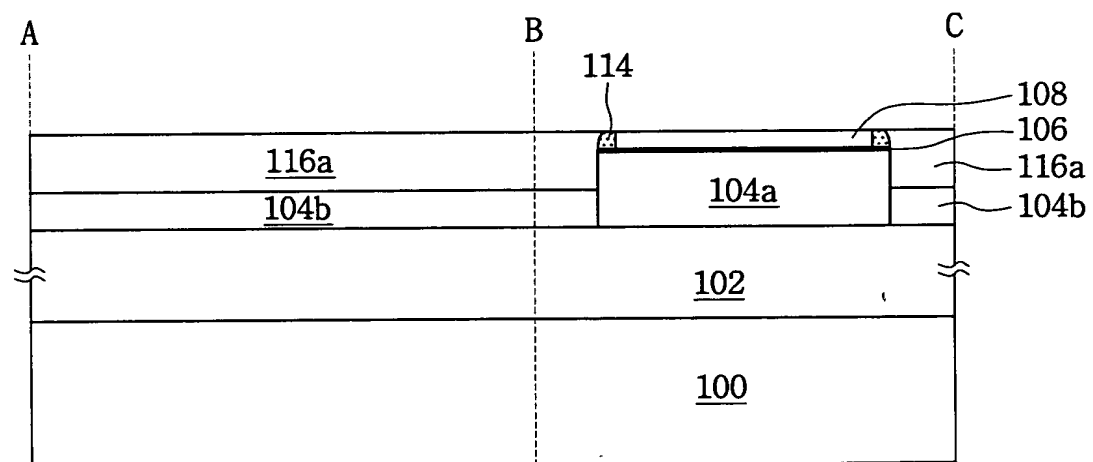


FIG. 4D



6/8

FIG. 4E

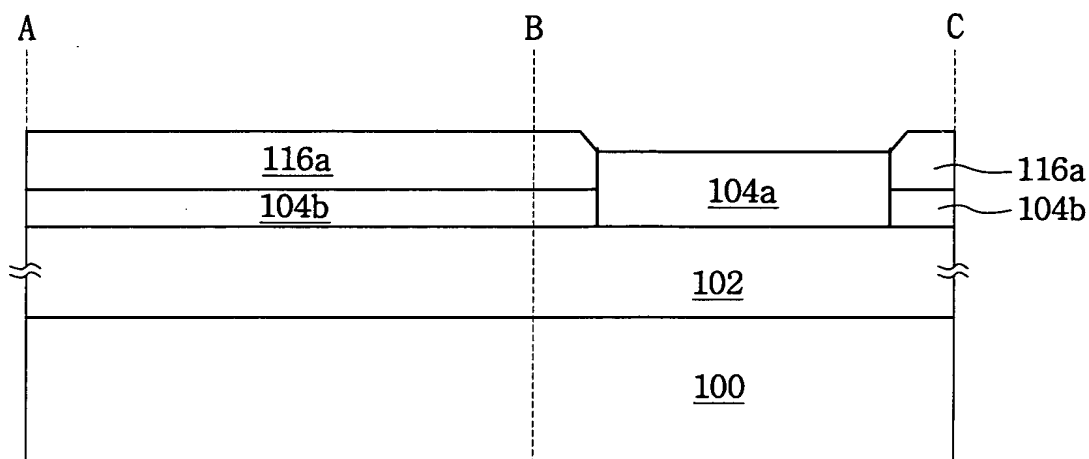
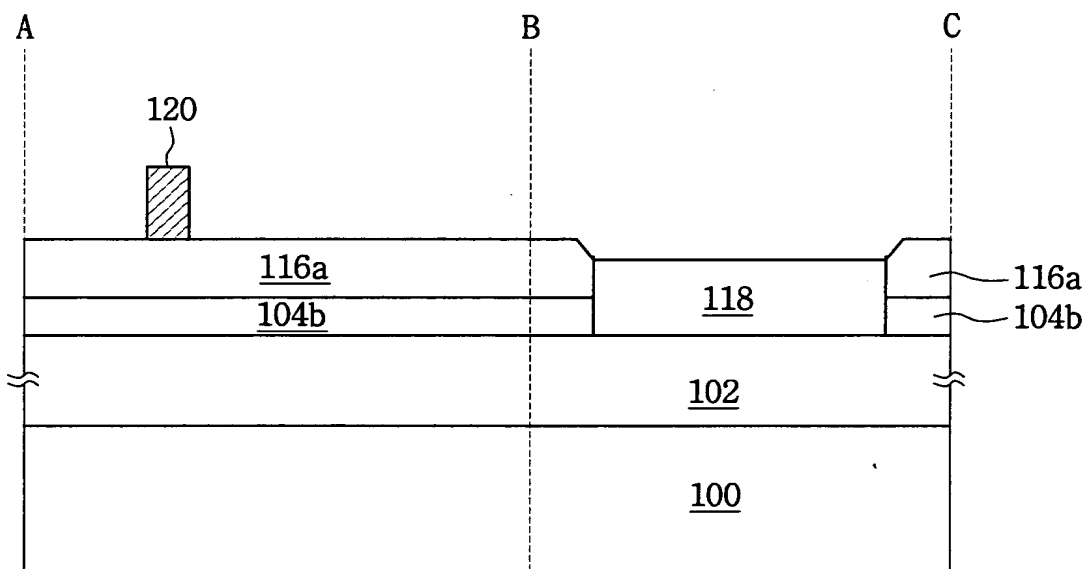


FIG. 4F



7/8

FIG. 4G

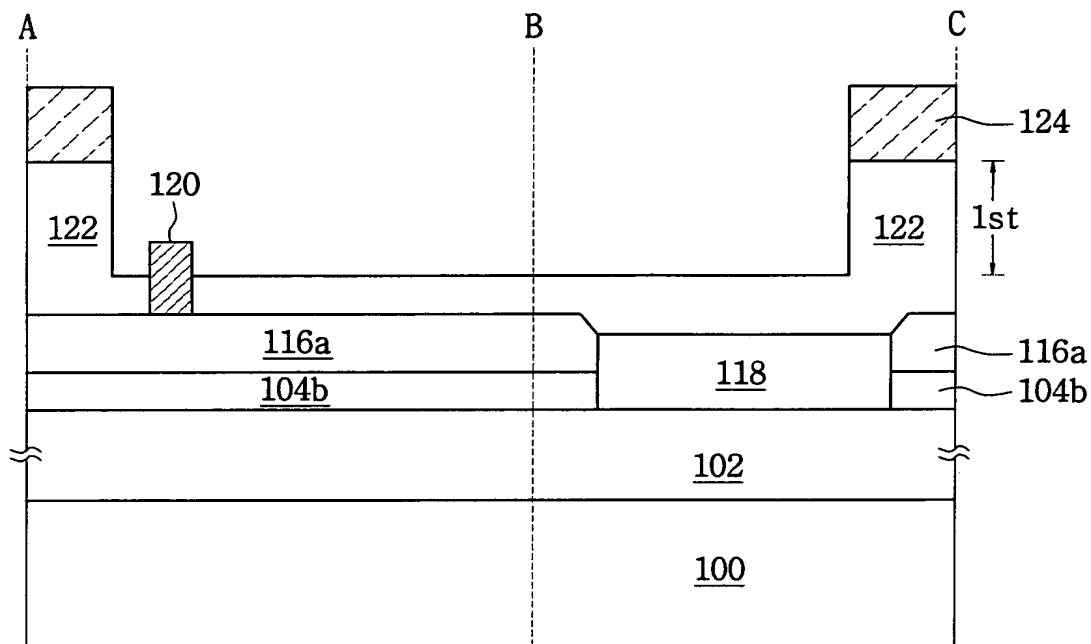
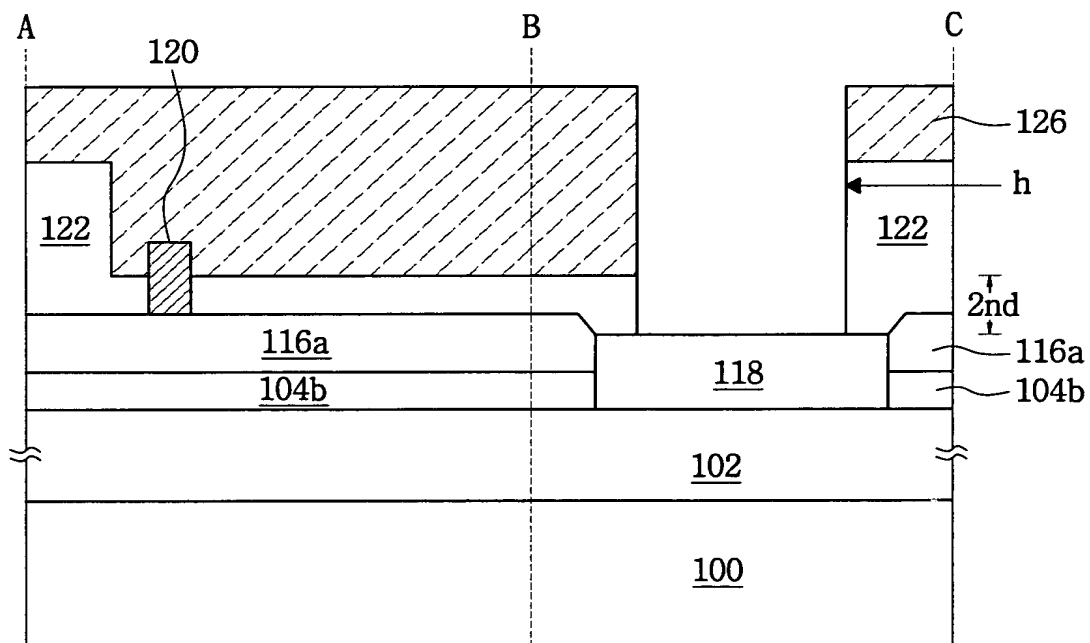


FIG. 4H



8/8

FIG. 4I

